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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/520,677	03/07/2000	Garry Z. Gu	56115534-120430	9129
46363	7590	06/14/2005		
			EXAMINER	
			NGUYEN, STEVEN H D	
			ART UNIT	PAPER NUMBER
			2665	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/520,677	GU, GARRY Z.	
	Examiner	Art Unit	
	Steven HD Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 February 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) _____ is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-6, 10-13, 15-27, and 31-36 is/are rejected.
 7) Claim(s) 7-9, 14 and 28-30 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 10-13, 15-27, and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsson et al. (US 6,172,963) in view of Caldara et al. (US 5,978,359) and Hunt et al. (US 6,249,819).

Regarding claims 1, 6, 10, 11, 13, 15, 18-21, 31, 32 and 34-36, Larsson discloses a credit-based flow control system for a switching network with input and output buffers. The input and output buffers meet the limitation of first and second stage port processors as in the present invention. The system takes into account the degree of fullness of the output buffers when determining how many cells (credits) can be sent from each input port. This process is called "giving credit" (col. 3, lines 21-30). With intelligence in the switch, it can be determined which output ports are able to receive cells (col. 4, lines 45-55). In the preferred embodiment, Larsson discloses a control unit (20) located in the switch core (8) for performing the intelligence. However, the intelligence may also be located outside the switch core and incorporated into the input buffers. In this case, the input ports would read the degree of fullness of the output buffers and calculate how many cells can be sent (col. 5, lines 12-23). This description meets the limitation of an integrator block in a first stage port processor, as in the present application. The limitation of neighboring integrator blocks is met by Larsson in that calculating the number of

cells to be sent to a particular output buffer includes determining which input ports should be allowed to send cells if several input ports are competing for the output buffer (col. 5, lines 31-36). Larsson also discloses determining which input ports are allowed to send cells based on priority classification (col. 5, lines 31-40). Thus, a higher priority input will be granted a greater number of credits, and some input must have the highest number of credits during each interval. It is obvious to send a cell through the input port with the highest number of grant credits if it is associated with a high priority connection. Larsson shows input ports (2-4) and output ports (5-7) in equal numbers, thus meeting the limitation of corresponding integrator blocks (Figure 3).

Larsson fails to expressly disclose sending a token bit from a second stage port processor to the neighboring first stage port processors in response to receiving a data packet at the second stage port processor. Caldara discloses a switching architecture that includes a first set of port processors, called To Switch Port Processors (TSPP) (14) and a second set of port processors, called From Switch Port Processors (FSPP) (16). These sets of TSPP'S and FSPP'S can be constructed as first and second stages in the switch, respectively. Caldara also discloses a feedback message (30) that provides an indication of buffer status at the output port. To provide efficient flow control, the feedback message from the output port to the input port includes several sub-type messages, including an ACCEPT/ REJECT bit (col. 5, line 64 - col. 6, line 14). This bit is considered to provide the function of the token bit of the applicant's invention. Caldara discloses it is determined if the output buffers become filled to a threshold level when sending the feedback message in order to prevent cell loss (col. 4, lines 37-53). it is obvious that some component must be present to count the number of cells in the output buffers and compare them to a threshold level in order to provide the functionality disclosed in the cited passage. This

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functionality in Caldara meets the limitation of a statistic block as described in the present application. Hunt discloses a Quantum Flow Control method wherein a downstream element may grant a certain number of credits to an upstream element, thus granting that upstream element permission to transmit to the downstream element, without any request from the upstream element (col. 3, lines 36-62). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use the feedback message of Caldara in combination with the credit based flow control system of Larsson to provide a switch that selectively sends data from a first stage to a second stage in accordance with the fullness or availability of each output buffer in the second stage. The feedback message of Caldara would notify the intelligent input ports in the first stage of Larsson as to the availability of the output buffers in order to calculate the credit given to each input port. It also would have been obvious to provide the feedback message of Caldara without receiving a request from a first stage, as in Hunt. One of ordinary skill in the art would have been motivated to send a message like the ACCEPT/REJECT bit of Caldara in the invention of Larsson in order to provide the input ports with the flow control information necessary to calculate the number of credits. One of ordinary skill in the art would have been motivated to do this without receiving a request from the input ports of Larsson in order to create a more efficient switching network.

Regarding claims 2, 3, 22 and 23, Larsson discloses multiple input ports. The teaching above provides a description for the incorporation of intelligence into the input port. This description provides for an equivalent to neighboring integrator blocks.

Regarding claims 4, 5, 12, 16, 17, 24-27 and 33, Larsson discloses that the number of cells (credits) that can be sent are calculated for a time interval and depend on the number of

cells already in the output buffers (col. 3, lines 45-58). Depending on the fullness of the output buffers from interval to interval, that the number of credits will change. This effectively achieves the process of incrementing and decrementing credits between time intervals.

Allowable Subject Matter

3. Claims 7-9, 14, and 28-30 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed 2/7/05 have been fully considered but they are not persuasive.

In response to pages 3-4, the applicant states that Larson fails to suggest an intelligence "control unit" could be incorporated into the input buffers. In reply, it has been held that there would be no invention in shifting the location parts, *In re Japikse*, 86 USPQ 70 (CCPA 1950). In this case, shifting the intelligent into another part of switch; the operation of the switch would not thereby be modified. Furthermore, the applicant states that Larson does not disclose a control unit in detail. In reply, In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the detail of integrator as showed in the figures 2-5) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the

specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to page 4, the applicant stated that Caldara does not meet the limitation of the claims because the accept/reject bit is performed in two steps. In reply, the second step which is a reply message which reads on a token bit message. Therefore, the teaching of Caldara performs the statistics block of the claim.

In response to pages 4-5, the applicant states that Hunt fails to disclose a token bit message transmitted in response to receive a data packet. In reply, Hunt discloses a method and system for using Credit based method for notifying the source node how many packets that the source node can transmit. The credit message is only generated after receiving some data packets from the source node.

5. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

6. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge

generally available to one of ordinary skill in the art or the nature of the problem to be solved. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992) and *In re Rouffet*, 149 F.3d 1350, 47, U.S.P.Q.2d 1453 (Fed. Cir. 1998). In this case, Larson discloses a method and system for forwarding the packets between the input and output buffer by using a well-known method such credit based to prevent congestion. Caldara discloses a method and system for transmitting a packet between input and output by using accept/reject message to prevent congestion. Hunt discloses a method and system for transmitting packets between the source and destination by using a well known and expected in the art such as credit based in order to prevent congestion. Since, the references disclose a method and system for preventing data loss and congestion. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to integrate the teaching into each other. The motivation would have been to create a more efficient switching network .

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

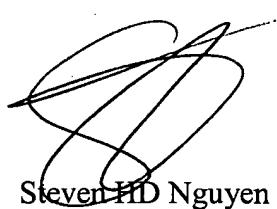
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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven HD Nguyen
Primary Examiner
Art Unit 2665
6/8/05